What is claimed is.

1. In the transmission of clocked time binary information signals with respect to a single reference level in a single information channel where said binary information signals are positioned between beginning and end phase shift signals,
an improvement for extraction of said phase shift signals comprising in combination:
means for arranging said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels, and,
means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal of said binary information signals that is greater than a low threshold that is less than the transition between said first and said second of said voltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels.

2. The improvement of claim 1 wherein said means for arranging said binary information signals in serial relation to first, second and third voltage levels includes a three level driver.

3. The improvement of claim 1 wherein said means for producing a new signal for each of said binary information signals that is based on an amplitude of a signal that is greater than a low threshold that is less than the transition between said first and said second of

said voltage levels and is less than a high threshold that is greater than the transition between said second and said third voltage levels includes a parallel reference amplifier circuit configuration with said high threshold level as one reference and said low threshold as the other reference level.

4. The improvement of claim 1 wherein said means for producing a new signal includes means for reflecting "current" and "previous" data in relating said new signal to said clocked time.

5. The improvement of claim 4 wherein said means for reflecting "current" and "previous" data is a look up table with said "previous" data provided from said "current" data with a one clock time cycle delay.

6. Clocked time binary information processing
comprising:
the arrangement of said binary information signals in serial relation to first, second and third voltage levels in said clocked time increments wherein each binary information signal is in two of said three voltage levels,
the producing of a new signal for each of said binary information signals that is within an amplitude range that is greater than a low threshold value less than a transition value between said first and said second of said voltage levels and is less than a high threshold value greater than a transition value between said second and said third voltage levels and the processing of said new signal in a differential amplifier between said high

and said low threshold values.

7. The processing of claim 6 including the additional step of further position processing of said new signal with respect to said clocked time.

8. The processing of claim 7 wherein said additional step is a signal positioning said new signal at the leading edge of said clocked time.

9. The removal of clock timing information and signal reshaping in binary data comprising the steps of:

arranging said binary data in serial binary bits,

passing each bit in relation to first, second and third voltage levels

wherein each binary bit signal extends into two of said voltage levels,

producing a new signal for each said binary bit that is within

an amplitude range that is greater than a low threshold value less than a transition value between said first and said second of said voltage levels and is less than a high threshold value greater than the transition value between said second and said third voltage levels, and,

positioning said new signal in relation to the leading edge of the next clock timing signal. (amended)

10. Data transmission apparatus for the transmission of binary data bits between first and second nodes,

comprising in combination:

an input stage operable to receive a binary information signal at a first transmission node,

said input stage being adapted to deliver a three voltage level driver signal voltage at an intermediate circuit node,

said three voltage level driver signal having serially,

in a first clock cycle increment, a first voltage level corresponding to the system reference voltage,

in a second clock cycle increment, a second and intermediate ,voltage level, and,

in a third clock cycle increment corresponding to a third and highest voltage level,

a comparator stage wherein said three level driver signal is compared in separate parallel first and second reference voltage comparison amplifiers each having said three level driver signal introduced at one input thereto,

said first reference voltage comparison amplifier having introduced at the remaining input a low threshold voltage that is higher than said reference voltage and is less than said intermediate voltage, and,

said second reference voltage comparison amplifier having introduced at the remaining input a high threshold voltage that is higher than said intermediate voltage and is less than said third voltage, and,

a binary information signal reconstruction stage responsive to output signals from said first and second comparison amplifiers ans adapted to establish the shape of an output binary bit signal.

11. The data transmission apparatus of claim 10 wherein said reconstruction stage includes delay means to position said output signal with respect to a clock for said data transmission system.

12. The data transmission apparatus of claim 11 wherein said reconstruction stage includes variable delay means operable to position said output signal within a window established by said clock for said data transmission system.

13. The data transmission apparatus of claim 12 wherein said reconstruction stage includes bistable circuit means establishing output signal turn on.

14. The data transmission apparatus of claim 12 wherein said reconstruction stage produces a new signal the magnitude of which is within an amplitude range that is greater than a low threshold value that is less than an intermediate voltage value that is between said first and said second of said voltage levels and is less than a high threshold value that is greater than said intermediate voltage and,

positioning said new signal in relation to the leading edge of the next clock timing signal.